What is claimed is:

1. An ultra small size vertical MOSFET (metal oxide semiconductor field effect transistor) device, comprising:

a silicon on insulator (SOI) substrate including a single crystal substrate, an oxide layer formed upon the single crystal substrate and a first single crystal silicon layer formed upon the oxide layer;

a first silicon conductive layer formed by doping an impurity of a high concentration into the first single crystal silicon layer;

a source contact, a channel and a drain contact formed on the first silicon conductive layer;

a gate insulating layer formed on the first silicon conductive layer, the source/drain contacts and the channel;

a second silicon conductive layer formed on the drain contact; and

a gate electrode formed on side walls of the channel.

2. The MOSFET device as recited in claim 1, further comprising:

an interlayer dielectric (ILD) layer formed on the gate electrode and the gate insulating layer; and

a source, a drain and a gate electrode interconnections to be connected with the source contact, a drain contact and the gate electrode.

3. The MOSFET device as recited in claim 1, the source/drain contacts and the channel are formed by annealing process after forming the second single crystal silicon layer and the second silicon conductive layer on the first silicon conductive layer.

4. The MOSFET device as recited in claim 3, the annealing process is carried out in a temperature ranging from approximately 700℃ to approximately 1,000℃ in a furnace selected from the group consisting of an electrical furnace and a rapid thermal annealing (RTA) furnace.

5. The MOSFET device as recited in claim 3, wherein the second single crystal silicon layer is formed by using a method selected from the group consisting of a chemical vapor deposition (CVD) and a molecular beam epitaxy (MBE) technique.

6. The MOSFET device as recited in claim 5, wherein the second conductive layer is formed using a material selected from the group consisting of an amorphous silicon and a poly-crystal silicon by the CVD technique.

7. The MOSFET device as recited in claim 1, wherein the gate insulating layer includes a material selected from the group consisting of a thermal oxide layer, a nitride layer, a CVD oxide layer and a CVD nitride layer.

8. A method for manufacturing an ultra small size vertical MOSFET device, the method comprising the steps of:

a) preparing an SOI substrate including a single crystal substrate, an oxide layer formed upon the single crystal substrate and a first single crystal silicon layer formed upon the oxide layer;

b) forming a first silicon conductive layer by doping an impurity of a high concentration into the first single crystal silicon layer;

c) forming a second single crystal silicon layer and a second silicon conductive layer on the first silicon conductive layer, wherein the second single crystal silicon layer has the impurity of a low concentration and the second silicon conductive layer has the impurity of a high concentration;

d) patterning the second silicon conductive layer and the second single crystal silicon layer vertically into a first predetermined configuration;

e) forming a gate insulating layer on the first silicon conductive layer, the second single crystal silicon layer and the second silicon conductive layer;

f) carrying out an annealing process to diffuse the impurities in the first silicon conductive layer and the second silicon conductive layer into the second single crystal layer, thereby forming a source contact, a drain contact and a vertical channel; and

g) forming a gate electrode on side walls of the

vertical channel, wherein the gate electrode encompasses the channel.

9. The method as recited in claim 8, wherein the step b) is carried out by using a method selected from the group consisting of an ion implantation and a vapor diffusion technique.

10. The method as recited in claim 8, wherein the step c) is carried out by using a method selected from the group consisting of a CVD technique and a MBE technique.

11. The method as recited in claim 8, wherein the second silicon conductive layer is formed using a material selected from the group consisting of an amorphous silicon and a poly-crystal silicon by the CVD technique.

12. The method as recited in claim 8, wherein the step d) is carried out using an etch mask by a dry etch process.

13. The method as recited in claim 12, wherein the etch mask includes a material selected from the group consisting of a photoresist, an oxide and a nitride layer.

14. The method as recited in claim 8, wherein the step f) is carried out in a temperature ranging from approximately 700℃ to approximately 1,000℃ in a furnace

selected from the group consisting of an electrical furnace and a rapid thermal annealing (RTA) furnace.

15. The method as recited in claim 8, wherein the gate insulating layer includes a material selected from the group consisting of a thermal oxide layer, a nitride layer, a CVD oxide layer and a CVD nitride layer.

16. The method as recited in claim 8, wherein the step g) includes the steps of:

g1) forming a third silicon conductive layer on the gate insulating layer;

g2) forming a first ILD layer on the third silicon conductive layer; and

g3) patterning the third silicon conductive layer and the first ILD layer into a second predetermined configuration, thereby obtaining the gate electrode.

17. The method as recited in claim 16, wherein the third conductive layer is formed by the CVD technique using a material selected from the group consisting of an amorphous silicon or a poly-crystal silicon.

18. The method as recited in claim 8, after the step g), further comprising the steps of:

h) forming a second ILD layer on the gate electrode and the gate insulating layer;

i) patterning the second ILD layer into a third predetermined configuration, thereby obtaining contact holes; and

j) depositing a metal or a silicon conductive layer in the holes, thereby forming a source, a drain and a gate electrode interconnections.